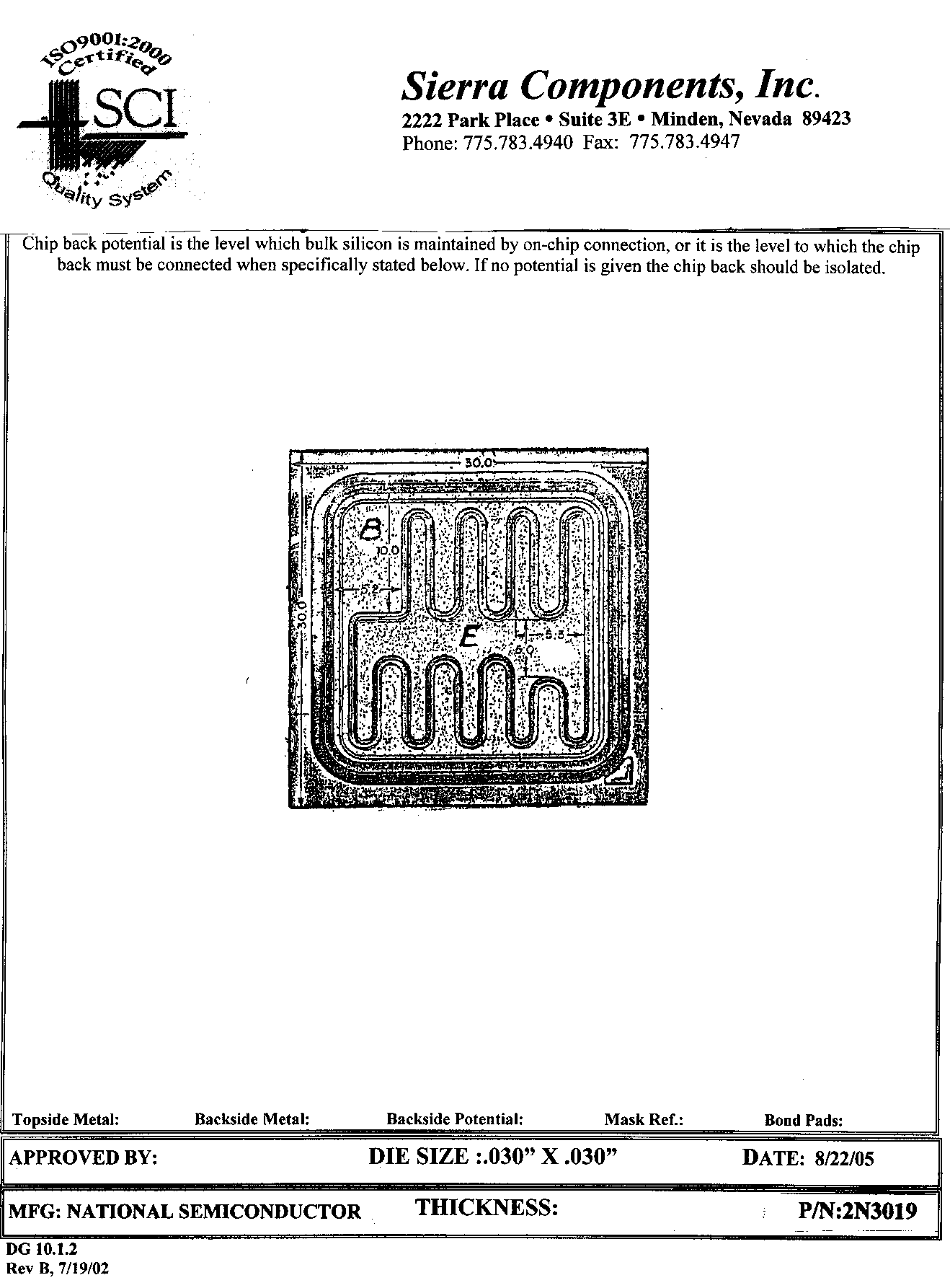
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.030”**



**B**

**E**

**.030”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: B = .005 x .009”**

**E = .004 x .005”**

**Backside Potential: COLLECTOR**

**APPROVED BY: DK DIE SIZE .030” X .030” DATE: 1/13/21**

**MFG: FAIRCHILD THICKNESS .006” P/N: MPSA05**

**DG 10.1.2**

#### Rev B, 7/1